Annulled Cycle Management on the TSC695

TSC695

Application Note

The aim of this application note is to provide TSC695 users with an overview of the annulled cycle management on the TSC695 processor. The indication of annulled cycle in the processor is output from the processor through the INULL signal. This information is required by some peripherals to correctly manage the transfers.

Depending on the memory area accessed, the TSC695 processor does not handle the annulled cycles in the same way.

References

- TSC695 SPARC® 32-bit Space Processor - User Manual

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Annulled Cycle

The TSC695 processor is able to indicate to its environment that nullified cycles are processed. The processor asserts its INULL signal to indicate that the current memory access is being nullified.

INULL is used to disable memory exception generation for the current memory access. This means that MDS (MDS*) and MEXC (MEXC*) are not asserted for a memory access in which INULL = 1.

INULL is asserted under the following conditions:

- During the second data cycle of any store instruction (including Atomic Load-Store) to nullify the second occurrence of the store address.
- On all traps, to nullify the third instruction fetch after the trapped instruction. For reset, it nullifies the error-producing address
- On a load in which the hardware interlock is activated
- On JMPL and RETT instructions

The INULL signal is asserted during the first clock cycle of the transaction that is annulled. Any standard access to memory (not nullified) is carried out with INULL deasserted in the first cycle of the access. The state of INULL during the rest of the operation is not significant.

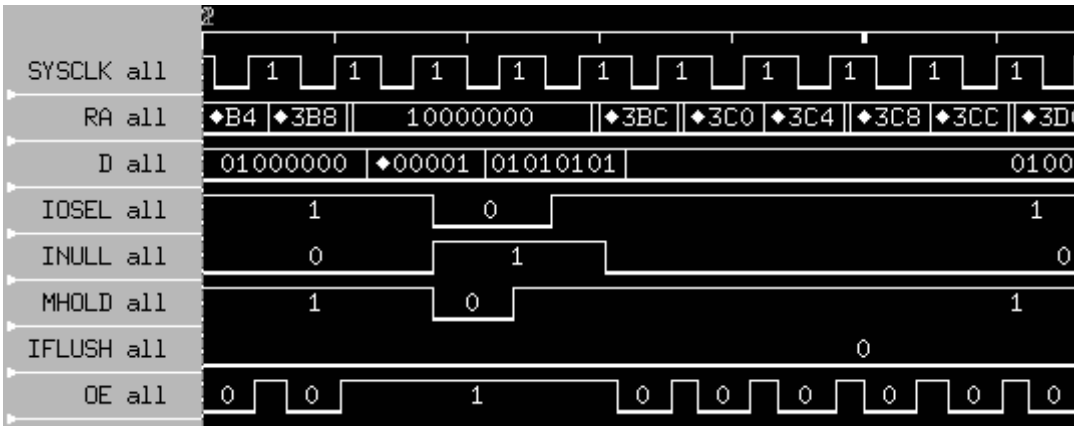
Note: 1. When more than 0 Wait States are programmed in the "Waitstate Configuration Register" for RAM, the INULL signal is asserted not only in the first clock cycle of the nullified instruction, but also throughout the previous memory access except the first clock period (If 3 W.S. are programmed for RAM read, and a nominal RAM fetch that lasts 4 clock cycle is executed followed by a nullified instruction, the INULL signal is asserted starting from the second clock cycle of the fetch cycle, and deasserted at the end of the first clock cycle of the nullified instruction).

INULL Management for RAM, ROM, I/O and Exchange Memory Areas

In the memory area controlled by dedicated chip selects, the TSC695 processor takes into account the INULL behaviour before the generation of the memory control signals. The transfers are not carried out during annulled cycles.

Figure 1 gives an example of store access during nominal activity while Figure 2 gives an example of INULL cycle management done directly by the TSC695 processor when a trap is taken.

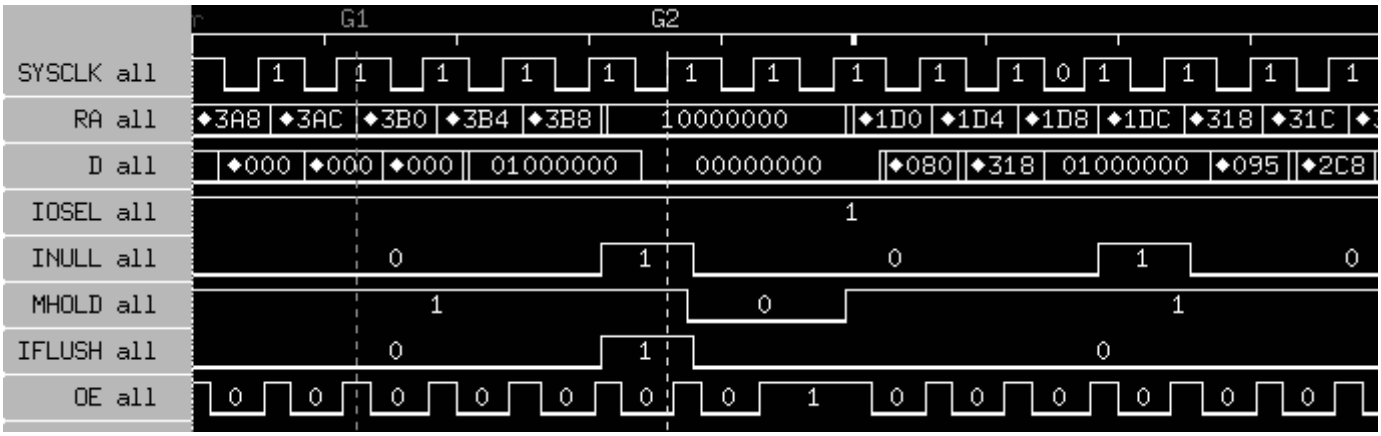
Figure 1. I/O Store Access - Nominal



During a normal Store access to IO spaces, IOsel signal is set to ‘0’. The chip select is correctly activated. The INULL signal is asserted in the second cycle of the transfer as expected for any store transfer.

The store access is successful.

Figure 2. I/O store access - Annulled



The ‘store’ access to the IO space is annulled by a trap occurence. IOsel signal remains high, no IO cycle is performed. The INULL signal is asserted in the first cycle of the transfer to be annulled. The cycle is correctly annulled by the processor.

Please note that during such an access, some extra OE* assertions are provided by the processor.

INULL Management for Extended Memory Areas

In the memory areas that are not controlled by dedicated chip selects, the user address decoder must take the INULL signal into account before allowing the access.

Except if it could have side effects, generally it would not be harmful to perform an unnecessary read operation (the processor does not sample any the data). But extra write cycles should be strictly forbidden. Such peripheral memory write operation could result in an invalid data storage, due to a floating data bus.

The following diagrams give examples of store access to a memory area where annulled cycles are not managed by the TSC695 processor.

Figure 3. Extended I/O Store Access - Nominal

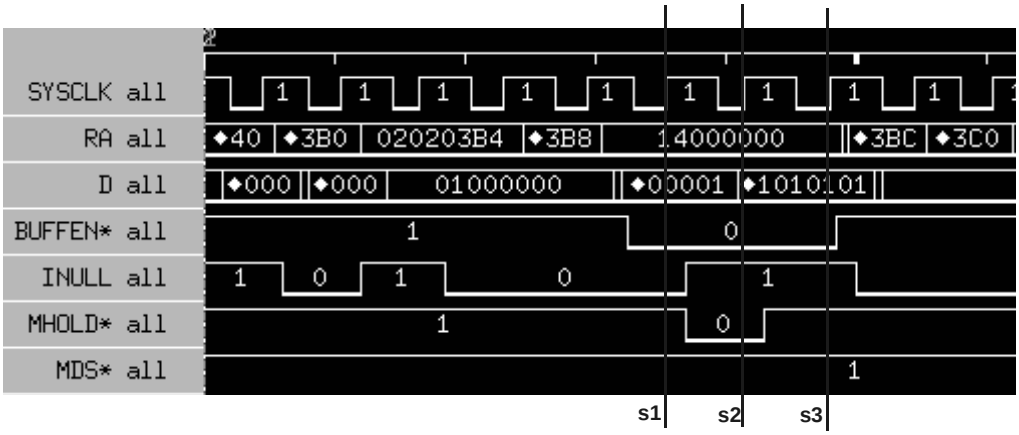
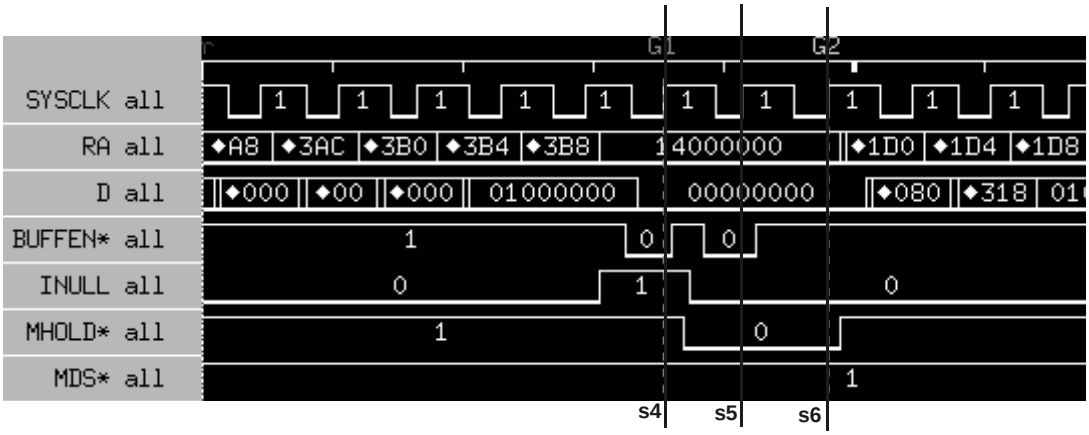


Figure 4. Extended I/O store access - Annulled



In Figure 4, the ‘store’ access to the Extended IO space is annulled by a trap occurence. The INULL signal is asserted in the first cycle of the transfer to be annulled. However, the address and control signal to be decoded by an external decoder are already available in the bus. If the external decoder does not take into account the INULL signal, a write cycle will be generated.

Please note that during such an access, the BUFFEN* behavior is different than in nominal case. Some extra BUFFEN* assertions are provided by the processor.

Consequently, if undecoded memory areas are used to perform I/O accesses, the INULL signal should be used to determine whether or not to execute the cycle. If the I/O can tolerate spurious reads, INULL decoding for these reads is not necessary.

Conclusion

As described in the previous pages, the TSC695 INULL behaviour depends on the memory area addressed. Two memory types can be identified:

- The processor directly handles the areas that are managed through dedicated chip selects.
- In case no chip select is provided by the processor, it is user ‘address and control’ decoder responsibility to manage the INULL signal before authorising the transfer. The decoder must verify the INULL signal status on the first cycle of the transfer to determine the validity of the transfer.

As a consequence, if an external address decoder is used for memory areas where the chip select signals are usually provided by the processor, it is the additional decoders responsibility to manage the INULL behaviour correctly.

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